## Chapter 10

## COM BINATIONAL CIRCUITS

## Introduction:

In a combinational logic circuit, the output is always dependent on the combination of its inputs and, if one of its input condition changes the state of the output also change. Combinational circuits do not have memory, so it does not store any information.

Types of combinational circuits:
Combine the logic gate like NAND, NOR or NOT gate we can build large number of combinational circuits. Some relevant combinational circuits are mentioned as follows:
(1) Adders
(2) Multiplexers
(3) De-multiplexers
(4) Decoders
(5) Encoder
(6) Converter
(7) Compartors.

## ADDERS CIRCUITS

Half adder: A logic circuit with two inputs and two outputs that can add two binary digits at a time, producing a sum and a carry, is called a half adder. It is called half adder because to complet binary addition we require two such half adders.


## Truth table of a half-adder:

| INPUT |  | OUTPUT |  |
| :---: | :---: | :---: | :---: |
| A | B | S | C |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 |

## Logical expression of HA:

From truth table we can write the expression for sum,

$$
\mathrm{S}=\mathrm{A} \overline{\mathrm{~B}}+\overline{\mathrm{A}} \mathrm{~B}=\mathrm{A} \oplus \mathrm{~B}
$$

The expression for carry, $\mathrm{C}=\mathrm{AB}$

## Half adder using XOR and AND gate only:



Half adder using NAND gate only:


## Half adder using NOR and AND gate only:



Half adder using NOR gate only:


## Full Adder (FA):

A half adder can handle only two bits at a time. But when adding two binary numbers we may have a carry bit coming from the column of lower significant bits. So, the adder circuit must be able to handle three digits at a time. For example, to add the binary numbers, $\mathrm{A}=\mathrm{A}_{\mathrm{n}} \mathrm{A}_{\mathrm{n}-1} \mathrm{~A}_{\mathrm{n}-2} \ldots . \mathrm{A}_{2} \mathrm{~A}_{1} \mathrm{~A}_{0}$ and $\mathrm{B}=\mathrm{B}_{\mathrm{n}} \quad \mathrm{B}_{\mathrm{n}-1}$ $B_{n-2} \ldots \ldots B_{2} B_{1} B_{0}$ the circuit must be able to add the nth bits $A_{n}$ and $B_{n}$ with carry $C_{n-1} 1$ generated from the addition of ( $n-1$ )th order bits. A full adder is a logic circuit with three inputs and two outputs that can add 3 bits at a time and give a sum and carry.

## Circuit symbol of Full Adder:



## Truth table of Full Adder:

| INPUTS |  |  | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{A}_{\mathrm{n}}$ | $\mathrm{B}_{\mathrm{n}}$ | $\mathrm{C}_{\mathrm{n}-1}$ | $\mathrm{~S}_{\mathrm{n}}$ | $\mathrm{C}_{\mathrm{n}}$ |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## Logic expression of full Adder:

From above truth table we can write the expression for sum:

$$
\mathrm{S}_{\mathrm{n}}=\mathrm{A}_{\mathrm{n}} \overline{\mathrm{~B}}_{\mathrm{n}} \overline{\mathrm{C}}_{\mathrm{n}-1}+\overline{\mathrm{A}}_{\mathrm{n}} \mathrm{~B}_{\mathrm{n}} \overline{\mathrm{C}}_{\mathrm{n}-1}+\overline{\mathrm{A}}_{\mathrm{n}} \overline{\mathrm{~B}}_{\mathrm{n}} \mathrm{C}_{\mathrm{n}-1}+\mathrm{A}_{\mathrm{n}} \mathrm{~B}_{\mathrm{n}} \mathrm{C}_{\mathrm{n}-1}
$$



From K-mapping we can write,

$$
\begin{aligned}
\mathrm{S}_{\mathrm{n}} & =\overline{\mathrm{A}}_{\mathrm{n}}\left[\mathrm{~B}_{\mathrm{n}} \oplus \mathrm{C}_{\mathrm{n}-1}\right]+\mathrm{A}_{\mathrm{n}}\left[\mathrm{~B}_{\mathrm{n}} \odot \mathrm{C}_{\mathrm{n}-1}\right] \\
& =\mathrm{A}_{\mathrm{n}} \oplus \mathrm{~B}_{\mathrm{n}} \oplus \mathrm{C}_{\mathrm{n}-1}
\end{aligned}
$$

The logic expression for carry

